

Appl. No. 10/508,745; Docket No. NL01 0251 US
Amdt. dated October 24, 2005
Response to Office Action Dated October 17, 2005

Amendments to the Claims

1. (*Original*) A semiconductor device comprising a substrate with a first and an opposed second side, at which first side a plurality of transistors and interconnects is present, which are covered by a protective security covering, which device is further provided with bond pad regions, characterized in that the protective security covering comprises a substantially non-transparent and substantially chemically inert security coating, and the bond pad regions are accessible from the second side of the substrate.
2. (*Previously Presented*) A semiconductor device as claimed in Claim 1, characterized in that
the bond pad regions are present on the first side of the substrate, and
the substrate is a silicon substrate, that is patterned as required for access to the bond pad regions.
3. (*Previously Presented*) A semiconductor device as claimed in Claim 1, characterized in that a security layer is present at the second side of the substrate, which security layer leaves exposed the bond pad regions or any metallisation for access thereto.
4. (*Original*) A semiconductor device as claimed in Claim 1, characterized in that the bond pad regions protected against probing with antiprobe means.
5. (*Previously Presented*) A semiconductor device as claimed in Claim 1, characterized in that the security coating comprises a layer of TiO₂.
6. (*Original*) A semiconductor device as claimed in Claim 1, characterized in that the security coating is formed of multiple alternate layers, which alternate layers are sensitive to different etchants.
7. (*Original*) A carrier comprising a semiconductor device according to Claim 1.

Claims 8-10 (*Cancelled*)